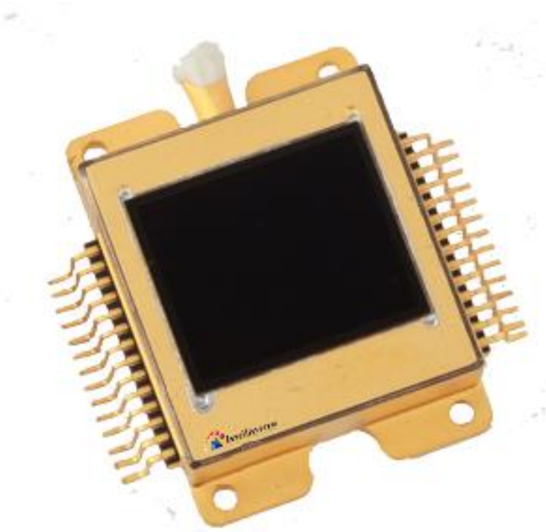
ThermalTronix

TT-1640DLD-DS

Long Wave Infrared Focal Plane Array

640×480 17um Uncooled Microbolometer

Issue D



Product Highlights

- *a-Si microbolometer*
- *640×480 focal plane array*
- *Pixel pitch 17um by 17um*
- *Hermetic Vacuum package*
- *Room temperature operation with TEC*
- *Military standard qualification*
- *On-chip temperature sensor*
- *Frame rate 25Hz～50Hz*
- *Single or double analog output*
- *Frame size selectable*
- *Image flip controllable*
- *Gain control selectable*

Contents

Table Lists

Figure Lists

Glossary

CMOS	Compatible Metal Oxide Semiconductor
CTIA	Capacitance Trans-Impedance Amplifier
ESD	Electrical Static Discharge
FPA	Focal Plane Array
IR	Infrared
LWIR	Long Wave Infrared
MEMS	Micro-Electro-Mechanical Systems
NC	Not Connected
NETD	Noise Equivalent Temperature Difference
ROIC	Read Out Integrated Circuit
TEC	Thermo-Electric Cooler

1 INTRODUCTION

This document describes the operation conditions and main performance specifications of an uncooled long wave infrared focal plane array detector with reference number of **TT-1640DLD-DS**.

The **TT-1640DLD-DS** infrared detector is based on CMOS-MEMS micro-bolometer technology. The detector is a 640×480 pixels array with pixel pitch of 17um by 17um. The detector is sensitive to the long-wave infrared (LWIR) spectral range of 8um～14um.

The **TT-1640DLD-DS** infrared detector is vacuum packaged with an incorporated non-evaporable getter to maintain long-term vacuum. The temperature of the detector is controlled with a thermo-electric cooler (TEC).

The **TT-1640DLD-DS** infrared detector is read-out row-by-row and can provide a single or a double analog output signal. The detector is typically operated under 25Hz～50Hz frame rate.

2 STRUCTURAL OVERVIEW

The **TT-1640DLD-DS** detector consists of following physical structures: hermetic sealed vacuum metal packaging, an IR filter window in the front of the packaging, a non-evaporable getter inside of the packaging to help maintain long-term vacuum level, the FPA chip with an integrated temperature sensor, a thermo-electric cooler (TEC) to stabilize the detector temperature.

2.1 Overall Dimension

The physical structure and overall dimensions of the detector packaging are described in the Appendix (sheet A to C).

2.2 Pin-out Diagram and List

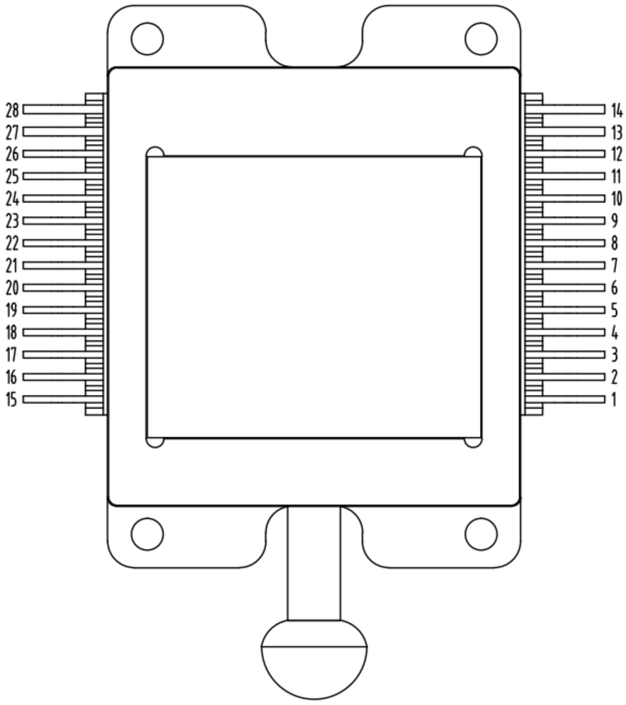
The pin-out diagram is presented in Figure 1, and the function of each pin is described in Table 1.

2.3 Infrared Filter

An infrared filter window is incorporated in the front side of the detector package.

The outline size of the IR filter is 19.0mm by 16.0mm, its thickness is 1.0mm. The optical interface detail is described in the Appendix (sheet C).

Symbol	PIN #
GETTER	28
TEC+	27
NC	26
NC	25
VOUT_EN	24
NC	23
DGND	22
SERIAL	21
SERDAT	20
DVDD	19
NC	18
RST	17
INT	16
MCLK	15



PIN #	Symbol
14	GETTER
13	TEC-
12	NC
11	VBS
10	VBB
9	TOUT
8	VPS
7	VPB
6	VREF
5	NC
4	AVDD
3	AGND
2	VOUT2
1	VOUT1

FIGURE 1 Detector Pin-out Diagram

TABLE 1 Detector Pin List

Pin Nr	Symbol	Function	Pin Nr	Symbol	Function
1	VOUT1	Video analog output 1	15	MCLK	Main clock
2	VOUT2	Video analog output 2	16	INT	Integration time
3	AGND	Analog ground	17	RST	Reset
4	AVDD	Analog supply	18	NC	Not connected
5	NC	Not connected	19	DVDD	Digital supply
6	VREF	Reference voltage	20	SERDAT	Serial link input data
7	VPB	Pixel biasing	21	SERIAL	Serial link input control
8	VPS	Pixel ground	22	DGND	Digital ground
9	TOUT	Temperature sensor	23	NC	Not connected
10	VBB	Blind pixel biasing	24	VOUT_EN	Effective display array
11	VBS	Blind pixel supply	25	NC	Not connected
12	NC	Not connected	26	NC	Not connected
13	TEC-	TEC-	27	TEC+	TEC+
14	GETTER	Getter	28	GETTER	Getter

Note: the NC pins can NOT be connected to any signal bus such as the ground etc.

2.4 Thermo-Electric Cooler

TABLE 2 Bias Requirements For The TEC

Pin Nr	Symbol	Absolute Max Rating
13	TEC-	Voltage: 4.3V Current: 3.0A Power: 7.0W
27	TEC+	

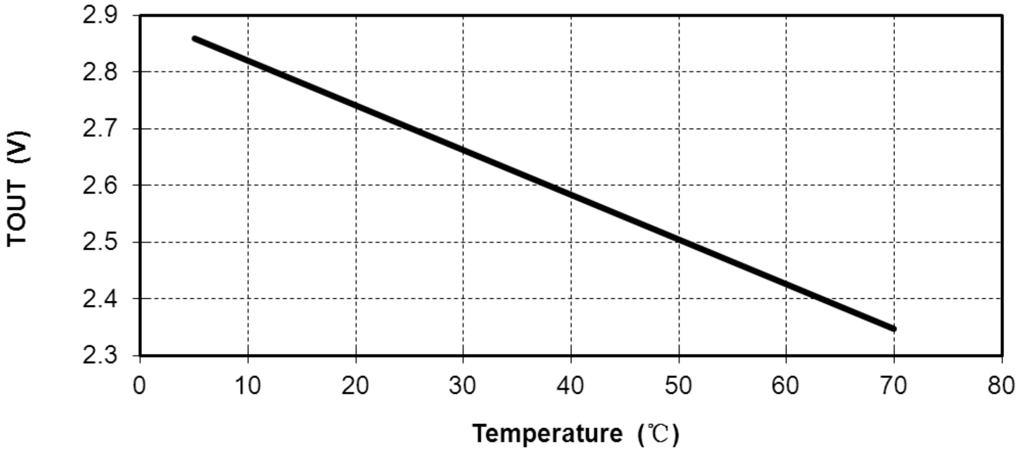
The temperature stabilization is required to be 10mK.

The stabilized temperature of the detector is typically set 10K～20K above the ambient temperature.

2.5 Temperature Sensor

A CMOS temperature sensor is integrated in the FPA ROIC chip. It provides an analog output voltage TOUT (PIN9) which is related directly to the temperature of the detector chip.

TOUT signal is also implemented into the video analog output (VOUT1 and VOUT2) at each line transition (see Figure 3).



A typical TOUT versus the detector chip temperature relationship is shown in Figure 2. The sensitivity of the temperature sensor is about -7.85 mV/K(Typical). TOUT is about 2.7 V for an FPA temperature of 25℃ (Typical).

FIGURE 2 Typical Temperature Sensor Output TOUT Characteristics

2.6 Vacuum and Getter

The **TT-1640DLD-DS** detector is required to operate under high vacuum condition. A non-evaporable getter is integrated in the packaging to maintain the long-term vacuum level. The getter can be electrically re-activated when the performance of the detector is degraded due to the vacuum level degradation. The getter activation is performed by supplying a constant current to the two pins of the getter as shown in Table 3. Re-active the getter by the customer is not recommended.

TABLE 3 Getter Re-activation Conditions

Pin Nr	Symbol	Current	Time
14/28	Getter	2.0A±0.1A	10min

2.7 Weight

The total weight of the **TT-1640DLD-DS** detector is less than 20g.

2.8 Operating Temperature

The operating temperature range of the **TT-1640DLD-DS** detector is from -40℃ to +60℃. A heat sink condition with typical thermal resistance of 4K/W is required between the packaging base plate and the ambient, especially when the detector is operated at the high end of the temperature range.

2.9 Storage Temperature

The storage temperature range of the **TT-1640DLD-DS** detector is from -40℃ to +85℃.

3 PERFORMANCE SPECIFICATION

A detector test report is provided with each delivered detector by the manufacturer which contains testing results of the responsivity, temporal NETD and operability.
The definitions of several parameters are further explained as following.

3.1 Responsivity

The detector responsivity is not a fixed performance specification parameter, the value supplied the test report is a measured value under the certain biasing and test conditions, and it is for information only.

3.2 Operability specification

3.2.1 Non-operating pixel

A pixel is defined as a “non-operating” if:

- its responsivity is less than 0.8x average responsivity or larger than 1.2x average responsivity;
- its NETD is larger than 1.5x average NETD;

3.2.2 Cluster

A cluster is defined as a group of at least 3x3 non-operating pixels adjacent.

3.2.3 Non-operating Row

A row is considered as non-operating if larger than 50% of the pixels are non-operating.

3.2.4 Non-operating Column

A column is considered as non-operating if larger than 50% of the pixels are non-operating.

3.2.5 Operability Specification

The operability of the delivered detector should meet the requirement in Table 4.

TABLE 4 Operability Specification

Non-operating row or column	0 non-operating row or column
Cluster	central zone of 160 x 120: ≤ 0 cluster other area: ≤ 2 clusters
Non-operating pixels	≤1%
Operability	≥99%

4 ELECTRICAL INTERFACE

4.1 Operation Bias Voltages

To properly operate the **TT-1640DLD-DS** detector, various bias voltages should be supplied to each pin as specified in Table 5.

TABLE 5 Operation Bias Conditions

Pin Nr	Symbol	Bias Type		Optimum Value	Range	Max Current	Max RMS Noise
3	AGND	Input	Fixed	0V	—	60mA	—
4	AVDD	Input	Fixed	5V±100mV	—	60mA	2uV(1Hz～1KHz) 5uV(1Hz～10KHz) 100uV(1Hz～10MHz)
6	VREF	Input	Fixed	Given in the test report	—	1mA	<100uV
7	VPB	Input	Tunable	Given in the test report	2V～5V	100uA	2uV(1Hz～1KHz) 5uV(1Hz～10KHz) 100uV(1Hz～10MHz)
8	VPS	Input	Fixed	0V	—	5mA	—
10	VBB	Input	Fixed	1.7V	—	100uA	2uV(1Hz～1KHz) 5uV(1Hz～10KHz) 100uV(1Hz～10MHz)
11	VBS	Input	Tunable	Given in the test report	2V～5V	5mA	2uV(1Hz～1KHz) 5uV(1Hz～10KHz) 100uV(1Hz～10MHz)
19	DVDD	Input	Fixed	5V±300mV	—	10mA	<100mV
22	DGND	Input	Fixed	0V	—	10mA	—

VPB、VBS can be adjusted to optimize the detector performance within the above range.

4.2 Pulse Voltage and Clock Diagram

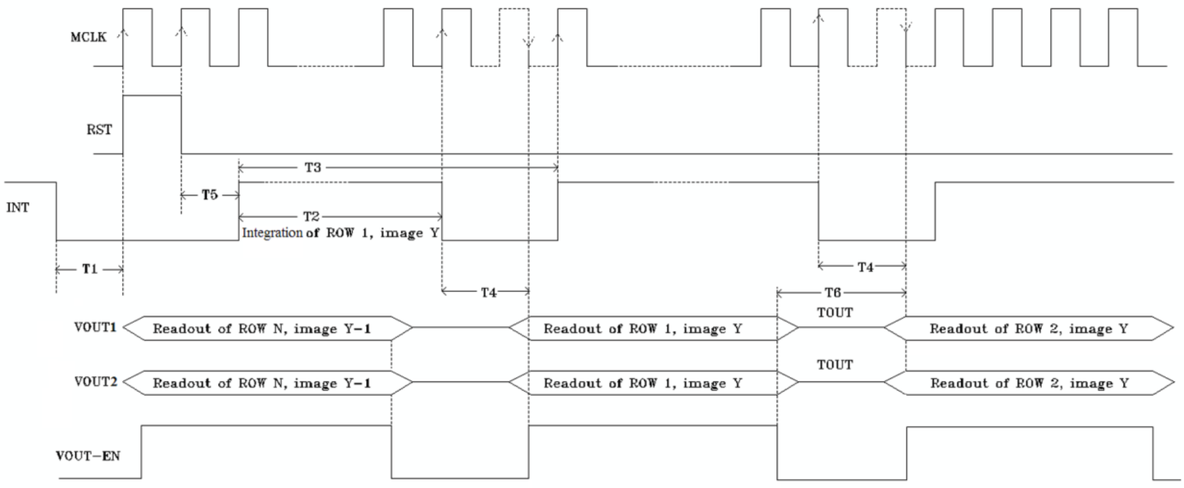
MCLK is the main clock of the ROIC, and it is a continuous pulse signal of 50% duty cycle. It synchronizes the operation of the whole circuit. The frequency of MCLK is 8.33 MHz for a 50 Hz frame rate in Double analog output mode (Typical).

RESET is used to reset the ROIC operation by forcing the integration of the signal on the first row of the FPA. It must not be repeated more than once per frame. RESET must change its state during a rising edge of MCLK.

INT is the integration signal of the ROIC. The high level of INT presents the integration time of a given row (T2 in Figure 3). The INT phase must be sent at each row. INT must change its state during the rising edges of MCLK. The detector is read row by row in a continuous frame rolling shutter mode. Row N integration and row N-1 readout run simultaneously. The analog output of effective pixels is present after 18.5 TMCLK of the falling edge of the INT (see figure 3).

TABLE 6 Pulse Voltages

Pin Nr	Symbol	Pulse Type		Low Level			High Level		
				Min	Typical	Max	Min	Typical	Max
15	MCLK	Input	5V TTL	-0.3V	0V	0.3V	4.7V	5V	5.5V
16	INT	Input	5V TTL	-0.3V	0V	0.3V	4.7V	5V	5.5V
17	RST	Input	5V TTL	-0.3V	0V	0.3V	4.7V	5V	5.5V
20	SERDAT	Input	5V TTL	-0.3V	0V	0.3V	4.7V	5V	5.5V



Single analog output： T1≥15TMCLK， 15TMCLK≤T2(Integration time)≤640 TMCLK, T3≥(640+17) TMCLK， T4=18.5TMCLK ，T5≥0

Double analog output： T1≥15TMCLK， 15TMCLK≤T2(Integration time)≤320 TMCLK, T3≥(320+17) TMCLK， T4=18.5TMCLK ，T5≥0

FIGURE 3 Clock Diagram for 640×480 Configuration

4.3 Serial Control

The serial control bus is developed for infrared imagers. The serial link (SERDAT: PIN #20) is used to write the required user data. And SERIAL (PIN #21) commands the serial link (SERDAT).

4.3.1 SERIAL

4.3.1.1 SERIAL=0V

a) SERDAT is off;
b) Single analog output(VOUT1);
c) CTIA capacitance is fixed to 14pF.

4.3.1.2 SERIAL=5V

When SERIAL=5V, SERDAT is available.
a) When SERDAT=0V, only VOUT1 single analog output, CTIA capacitance is fixed to 18pF;
b) When SERDAT is defined by 4.3.2, all the functions given by the serial link are available.

4.3.2 Serial Control Bus

4.3.3 SERDAT (PIN #20) is a 51 bits control signal defined as in Table 7. The main feature of the serial interface include：

a) Single analog output or double analog output: NBOUT
b) CTIA gain value: GAIN
c) Image flip: HFLIP、VFLIP
d) Windowing: SIZEA、SIZEB

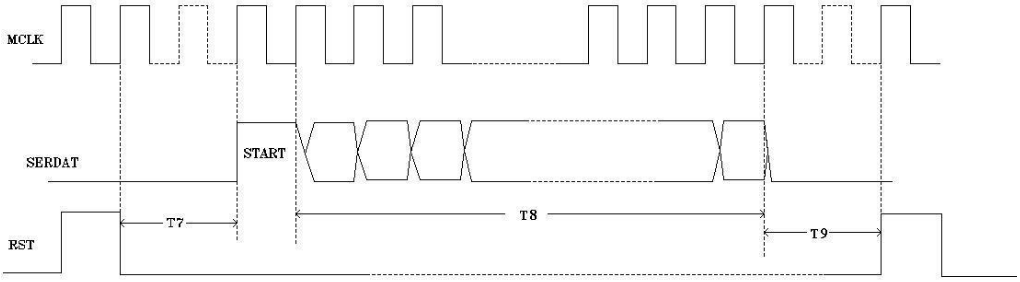
SERDAT can be applied by each frame or just once.

To activate the serial control bus, the first bit named START needs to be set at “1” i.e high level.

The clock frequency of SERDAT is governed by the Master Clock (MCLK). Data will be taken into account if START bit is at high level. Data must change during rising edge of MCLK and will be taken into account at the falling edge of the next RST. The timing diagram of SERDAT is shown in Figure 4.

TABLE 7 Serial Link Instruction

Position	**Length (in bit number)**	**Name**	**Format (binary/decimal)**	**Example**	
				Value	**Binary conversion**
1	1	START	Binary	1	1
2	1	Reserved	Binary	0	0
3	3	Reserved	Binary	0,0,0	000
4	1	NBOUT	Binary	1	1
5	3	GAIN	Binary	1,1,1	111
6	1	HFLIP	Binary	1	1
7	1	VFLIP	Binary	1	1
8	1	SIZE-A	Binary	1	1
9	1	SIZE-B	Binary	1	1
10	9	Y_{first}	Decimal	160	010100000
11	9	Y_{last}	Decimal	320	101000000
12	10	X_{first}	Decimal	160	0010100000
13	10	X_{last}	Decimal	320	0101000000



T7≥1TMCLK，T8=50TMCLK，T9≥1TMCLK

FIGURE 4 SERDAT Timing Diagram

4.3.2.1 Output Mode Control

The following table gives the output mode versus NBOUT value:

TABLE 8 Output Mode Control

NBOUT	Output mode
1	Single-end（VOUT1）
0	Double-end

Only VOUT1 is available in single output mode, while VOUT1 and VOUT2 are all available in double output mode.

4.3.2.2 Gain Control

The GAIN enable CTIA gain adaptation for specific operating conditions. The different avilable configurations are as following:

TABLE 9 CTIA Gain Control

Gain	Value	CTIA Capacitance (pF)
1.00	111	18
1.125	011	16
1.29	101	14
1.50	001	12
1.80	110	10
2.25	010	8
3.00	100	6
4.50	000	4

4.3.2.3 Image Flip

The image could be flipped in horizontal and vertical direction using HFLIP and VFLIP input, as described in Table 10.

TABLE 10 Image Flip Control

Scanning Direction	HFLIP	VFLIP
right→left/up→down	1	1
right→left/down→up	1	0
left→right/up→down	0	1
left→right/down→up	0	0

4.3.2.4 Windowing

Three different windows of interest are available: 640×480, 384×288 and 320×240 with the same optical center plus a user defined window determined by 2 opposite corner coordinates. The selection of the size is made by the serial link. The following table gives the size format versus the SIZEA and SIZEB values:

The user defined window need abide bellow rule(X-Y): Column defination: 160≤X≤640； Row defination: 1≤Y≤480.

TABLE 11 Format Size Control

FORMAT	SIZEA	SIZEB
640×480	1	1
384×288	1	0
320×240	0	1
User Defined	0	0

4.4 Output Characteristics

The detector contains some outputs, named VOUT1, VOUT2, TOUT and VOUT_EN.
VOUT1 and VOUT2 are the analog video output, their output arrangements are shown in Table 12. TOUT is the temperature sensor output. VOUT1, VOUT2 and TOUT are described in Table 13.

VOUT_EN is a digital output of 5V TTL. Its high level indicates the presence of valid data on the analog output (VOUT). And its low level indicates the presence of temperature sensor output TOUT.

Analog output VOUT and TOUT can be loaded by a resistance R ≥ 1MΩ in parallel with a capacitance C ≤ 10pF.

TABLE 12 Outputs arrangement

Single output mode	Double output mode	
VOUT1	VOUT1	VOUT2
Column 1 Row 1	Column 1 Row 1	Column 2 Row 1
Column 2 Row 1	Column 3 Row 1	Column 4 Row 1
…	…	…
Column M Row 1	Column(M-1) Row 1	Column M Row 1
Column 1 Row 2	Column 1 Row 2	Column 2 Row 2
Column 2 Row 2	Column 3 Row 2	Column 4 Row 2
…	…	…
Column M Row 2	Column(M-1) Row 2	Column M Row 2
Column 1 Row 3	Column 1 Row 3	Column 2 Row 3
Column 2 Row 3	Column 3 Row 3	Column 4 Row 3
…	…	…
…	…	…
Column M Row N	Column(M-1) Row N	Column M Row N

M is the column number and N is the row number. M=640, N=480 for 640×480 format.

TABLE 13 Outputs

Pin Nr	Symbol	Output Type		Range
1	VOUT1	Output	variable	0.4V～4.0V
2	VOUT2	Output	variable	0.4V～4.0V
9	TOUT	Output	variable	2.0V～3.3V

5 ENVIRONMENTAL CONDITIONS

TT-1640DLD-DS detector is GJB-qualified (MIL-STD equivalent). The detector qualification is performed on the basis of sampling from the manufactured products and is representative of the typical manufacturing technology level. The detector should be qualified to the climatic and mechanical environmental conditions as listed in Table 14.

TABLE 14 Environment Conditions

Nr	Item	Standard and Method
1	High temperature storage	GJB 1788 Method 2020
2	Low temperature storage	GJB 1788 Method 2040
3	Thermal Shocks	GJB 1788 Method 2010
4	Random vibration	GJB 1788 Method 2080
5	Shocks	GJB 1788 Method 2070

6 DELIVERY

6.1 Packing

During transportation, the detector is placed into a plastic box and wedged with conductive foam, a testing report is delivered together with each detector.

6.2 Storage

Detectors should be stored at conditions: temperature at -10℃～40℃, relative humidity is less than 70%, dry and non-corrosive environment.

6.3 General Recommendations

Specific care should be taken in handling the **TT-1640DLD-DS** detector:

a) Electrostatic discharge (ESD) protection

b) Avoid directing the detector directly towards the sun, especially in the case the detector is mounted with a lens

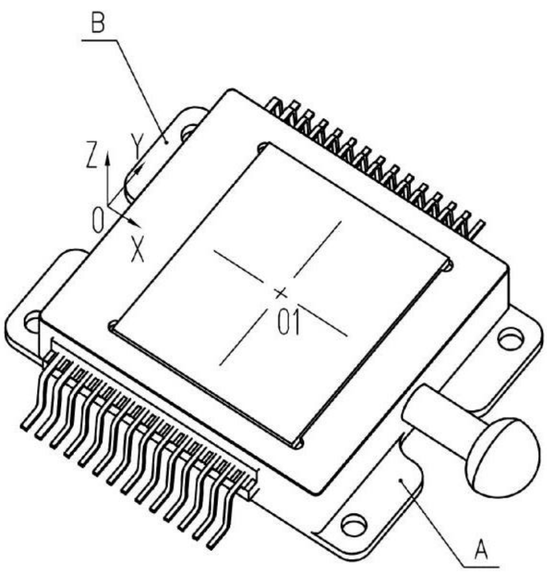
7 APPENDIX

a) Sheet A： General View

b) Sheet B： Mechanical Interface

c) Sheet C： Optical Interface

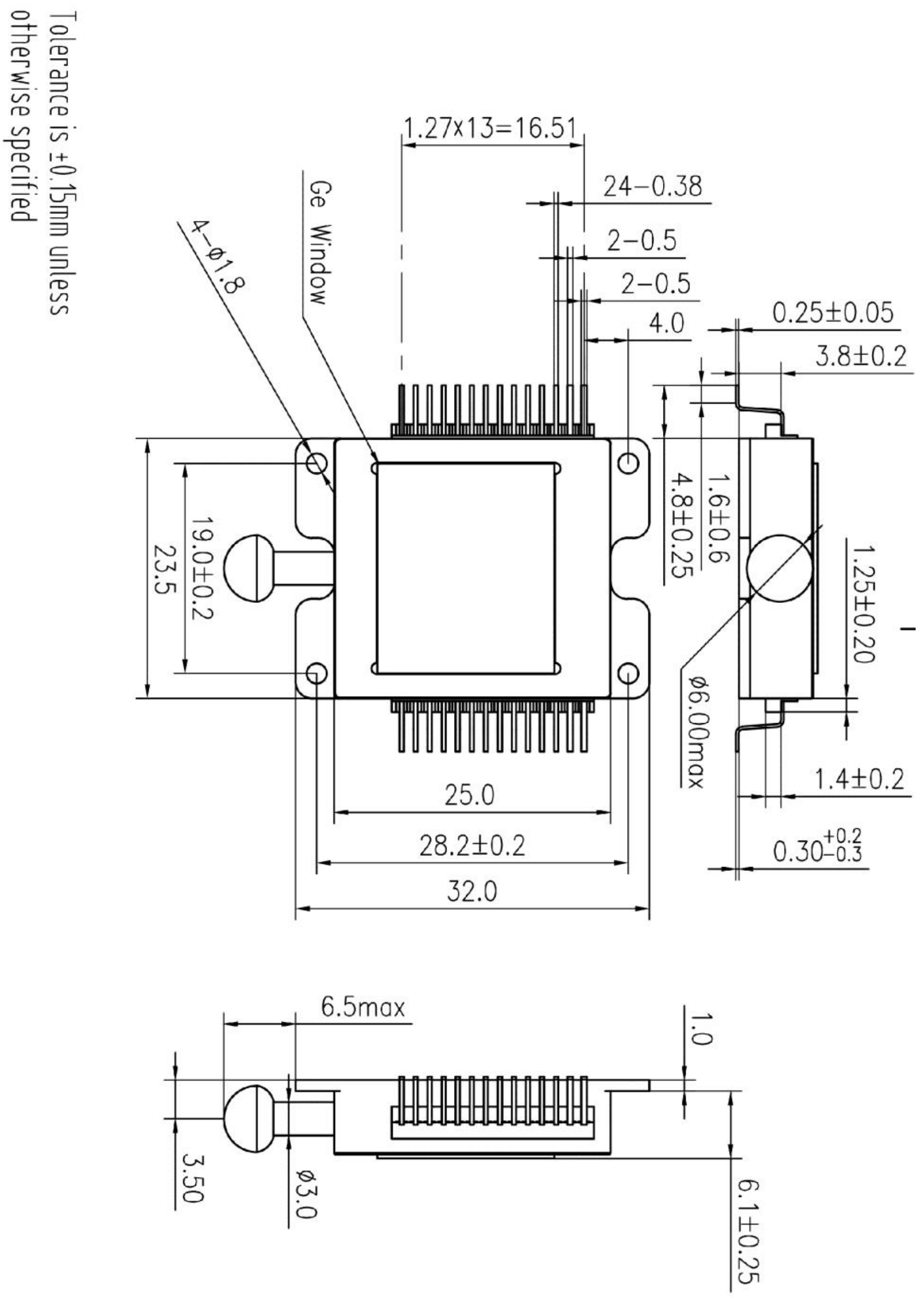
Sheet A General View



NOTE

1-Mechanical reference OXYZ are materialised by:
XY: Mechanical Mounting surface (A plane)
X: Symmetry axis of the structure
Y: Perpendicular to X axis through line B
Z: Normal to XY plane
0: XYZ axis center
2-01: Optical plane center

Sheet B Mechanical Interface



Sheet C Optical Interface