ThermalTronix
TT-1384BLD-DS
Long Wave Infrared Focal Plane Array

384×288 35um Uncooled Microbolometer

Issue E
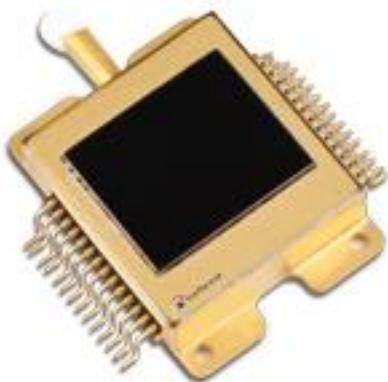
Product Highlights

- *a-Si microbolometer*   - *On-chip temperature sensor*

- *384×288 focal plane array*   - *Frame rate 30 – 60 Hz*

- *Pixel pitch 35um by 35um*   - *Frame size selectable*

- *Hermetic vacuum package*   - *Single analog output*

- *Room temperature operation with TEC*   - *Image flip controllable*

- *Military standard qualified*   - *Gain control selectable*

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Glossary

CMOS	Compatible Metal Oxide Semiconductor
CTIA	Capacitance Trans-Impedance Amplifier
ESD	Electrical Static Discharge
FPA	Focal Plane Array
IR	Infrared
LWIR	Long Wave Infrared
MEMS	Micro-Electro-Mechanical Systems
NC	Not Connected
NETD	Noise Equivalent Temperature Difference
ROIC	Read Out Integrated Circuit
TEC	Thermo-Electric Cooler

1 INTRODUCTION

This document describes the operation conditions and main performance specifications of an uncooled long wave infrared focal plane array detector with reference number of **TT-1384BLD-DS**.

The **TT-1384BLD-DS** infrared detector is based on CMOS-MEMS micro-bolometer technology. The detector is a 384×288 pixels array with pixel pitch of 35um by 35um. The detector is sensitive to the long-wave infrared (LWIR) spectral range of 8um～14um.

The **TT-1384BLD-DS** infrared detector is vacuum packaged with an incorporated non-evaporable getter to maintain long-term vacuum. The temperature of the detector is controlled with a thermo-electric cooler (TEC).

The **TT-1384BLD-DS** infrared detector is read-out row-by-row and provides a single analog output signal. The detector is typically operated under 30Hz～60Hz frame rate.

2 STRUCTURAL OVERVIEW

The **TT-1384BLD-DS** detector consists of following physical structures: hermetic sealed vacuum metal packaging, an IR filter window in the front lid of the packaging, a non-evaporable getter inside of the packaging to help maintaining long-term vacuum level, a temperature sensor integrated in the FPA ROIC chip, a thermo-electric cooler (TEC) to stabilize the detector temperature.

2.1 Overall Dimension

The physical structure and overall dimensions of the detector packaging are described in the Appendix (sheet A to C).

2.2 Infrared Filter

An IR filter window is incorporated in the front side of the detector package.

The outline size of the IR filter is 19.0mm by 16.0mm, its thickness is 1.0mm. The optical interface detail is described in the Appendix (sheet C).

2.3 Pin-out Diagram and List

The pin-out diagram is presented in Figure 1, and the function of each pin is described in Table 1.

Symbol	PIN #
GETTER	28
TEC+	27
DVSS	26
DVDD	25
SIZE	24
S3	23
NC	22
S2	21
VFLIP	20
S1	19
HFLIP	18
RST	17
RCLK	16
CCLK	15

PIN #	Symbol
14	GETTER
13	TEC-
12	TOUT
11	VBS
10	VPS
9	NC
8	NC
7	NC
6	VBB
5	VPB
4	VREF
3	AVSS
2	VOUT
1	AVDD
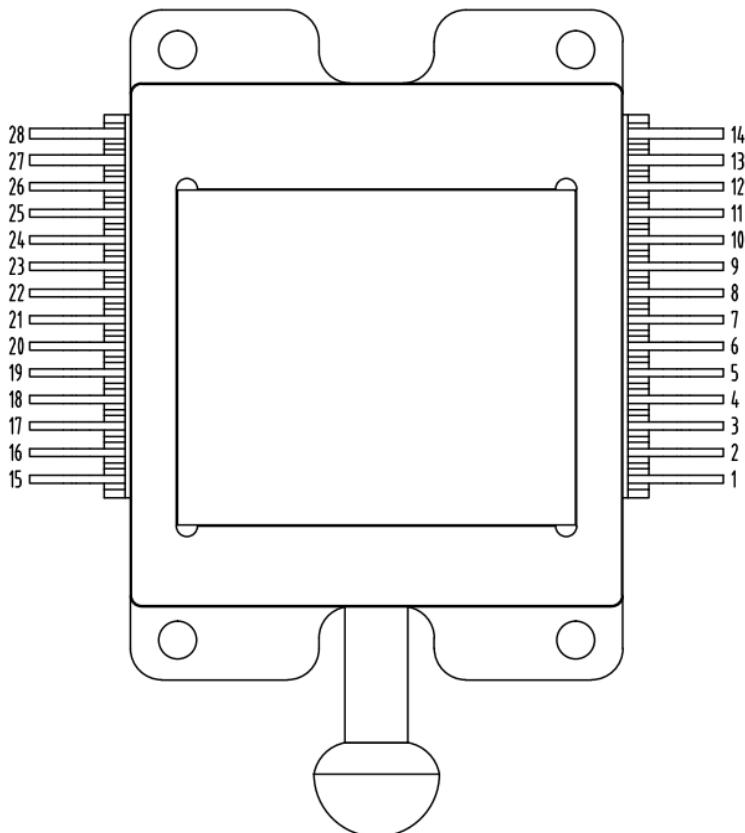
figure 1 detector pin out diagram

TABLE 1 Detector Pin List

Pin Nr	Symbol	Function	Pin Nr	Symbol	Function
1	AVDD	Analog supply	15	CCLK	Pixel synch
2	VOUT	Video analog output	16	RCLK	Line synch
3	AVSS	Analog ground	17	RST	Reset
4	VREF	Reference voltage	18	HFLIP	Image horizontal flip
5	VPB	Pixel biasing	19	S1	Gain control
6	VBB	Blind pixel biasing	20	VFLIP	Image vertical flip
7	NC	Not connected	21	S2	Gain control
8	NC	Not connected	22	NC	Not connected
9	NC	Not connected	23	S3	Gain control
10	VPS	Pixel ground	24	SIZE	Frame array size
11	VBS	Blind pixel supply	25	DVDD	Digital supply
12	TOUT	Temperature sensor output	26	DVSS	Digital ground
13	TEC-	TEC-	27	TEC+	TEC+
14	GETTER	getter	28	GETTER	getter

PINs marked NC can **NOT** be connected to the ground or any other type of supply bus

2.4   Thermo-Electric Cooler

A single-stage thermo-electric cooler (TEC) is integrated into the metal package to stabilize the temperature of the detector chip. The TEC has two input pins as described in Table 2.

TABLE 2 Bias requirements for the TEC

Function	Pin Nr	Absolute Max Rating	
TEC+	27	Voltage: 4.3V	Current: 3.0A
TEC-	13	Power: 7.0W	

The temperature stabilization is required to be 10mK.

The stabilized temperature of the detector is typically set 10K – 20K above the ambient temperature.

2.5 Temperature Sensor
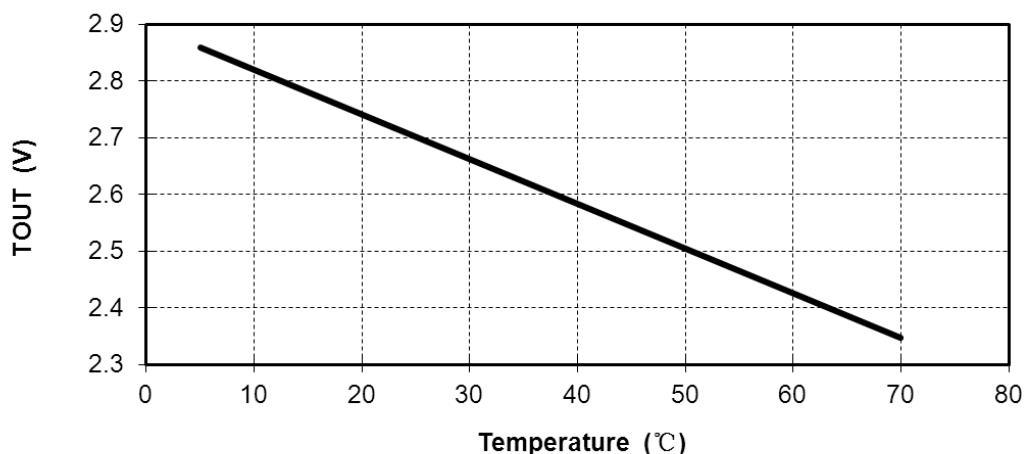
A CMOS temperature sensor is integrated in the FPA ROIC chip. It provides an analog output voltage TOUT which is related directly to the temperature of the detector chip.

A typical TOUT versus the detector chip temperature relationship is shown in Figure 2. The sensitivity of the temperature sensor is about -7.85mV/K. TOUT is about 2.70V for an FPA temperature of 25℃.

**FIGURE 2 Typical temperature sensor output TOUT
characteristics**

2.6 Vacuum and Getter

The **TT-1384BLD-DS** detector is required to operate under high vacuum condition, which is provided by the hermetic metal packaging. A non-evaporable getter is integrated in the packaging to maintain the long-term vacuum level. The getter can be electrically re-activated when the performance of the detector is degraded due to the vacuum level degradation. The getter activation is performed by supplying a constant current to the two pins of the getter as shown in Table 3. Re-active the getter by the customer is not recommended.

TABLE 3 Getter re-activation conditions

Function	Pin Nr	Current	Time
Getter +/-	14/28	2.0A±0.1A	10min

2.7 Weight

The total weight of the **TT-1384BLD-DS** detector is less than 20g.

2.8 Operating Temperature

The operating temperature range of the **TT-1384BLD-DS** detector is from -40℃ to +60℃. A heat sink condition with typical thermal resistance of 4K/W is required between the packaging base plate and the ambient, especially when the detector is operated at the high end of the temperature range.

2.9　Storage Temperature

The storage temperature range of the **TT-1384BLD-DS** detector is from -40℃ to +85℃.

3 PERFORMANCE SPECIFICATIONS

A detector test report is provided with each delivered detector by the manufacturer which contains testing results of the responsivity, temporal NETD and operability.
The definitions of several parameters are further explained as following.

3.1　Responsivity

The detector responsivity is not a fixed performance specification parameter, the value supplied in the test report is a measured value under certain biasing and test conditions.

3.2　Operability specifications

3.2.1　Non-operating pixel

A pixel is defined as a "non-operating" if:
- its responsivity is less than 0.8x average responsivity or larger than 1.2x average responsivity; or
- its NETD is larger than 1.5x average NETD;

3.2.2　Non-operating Row

A row is considered as non-operating if more than 50% of the pixels in the row are non-operating.

3.2.3　Non-operating Column

A column is considered as non-operating if more than 50% of the pixels in the column are non-operating.

3.2.4　Operability Specifications

The operability of the delivered detector should meet the requirement in Table 4.

TABLE 4 Operability Specification

non-operating row or column	0
non-operating pixels	≤1.0%
Operability	≥99%

4 ELECTRICAL INTERFACE

4.1　Operation Bias Conditions

To properly operate the **TT-1384BLD-DS** detector, various bias voltages should be supplied to each pin as specified in Table 5.

TABLE 5 Operation bias conditions

Pin	Symbol	Bias type		Optimum	Range	Max curre	Max RMS noise
1	AVDD	input	fixed	—	5V	50mA	2uV(1Hz to 1KHz) 5uV(1Hz to 10KHz) 100uV(1Hz to
3	AVSS	input	fixed	—	0V	50m	—
4	VREF	input	fixed	—	2.4	1mA	100uV(1Hz to
5	VPB	input	tunable	Given in the test	2V - 5V	100uA	2uV(1Hz to 1KHz) 5uV(1Hz to 10KHz) 100uV(1Hz to
6	VBB	input	fixed	—	1.7 V	100uA	2uV(1Hz to 1KHz) 5uV(1Hz to 10KHz) 100uV(1Hz to
1	VPS	input	fixed	—	0V	5mA	—
11	VBS	input	tunable	Given in the test	2V - 5V	5mA	2uV(1Hz to 1KHz) 5uV(1Hz to 10KHz) 100uV(1Hz to
2	DVDD	input	fixed	—	5V	5mA	10mV(1Hz to
2	DVSS	input	fixed	—	0V	5mA	—

VPB、VBS can be adjusted to optimize the detector performance within the above range

4.2   Pulse Voltage and Clock Diagram

The sequence of the detector operation is controlled by the three pulse voltages CCLK, RCLK and RST. The pulse voltage condition is described in Table 6.

A proper clock sequence for the three pulses should be supplied to operate the detector, which is recommended in Figure 3 for 384×288 configuration and in Figure 4 for 320×240 configuration. The rise and fall times of the three pulse voltages should be less than 10ns. Charge integration time is equal to the time duration of the low level of RCLK.

TABLE 6 Pulse Voltage Conditions

Pin	Symbol	Bias type		Low			High		
				Min	Typica	Max	Min	Typica	Max
1	CCL	inpu	5V TTL	-	0V	0.3V	4.7V	5V	5.5V
1	RCL	inpu	5V TTL	-	0V	0.3V	4.7V	5V	5.5V
1	RST	inpu	5V TTL	-	0V	0.3V	4.7V	5V	5.5V
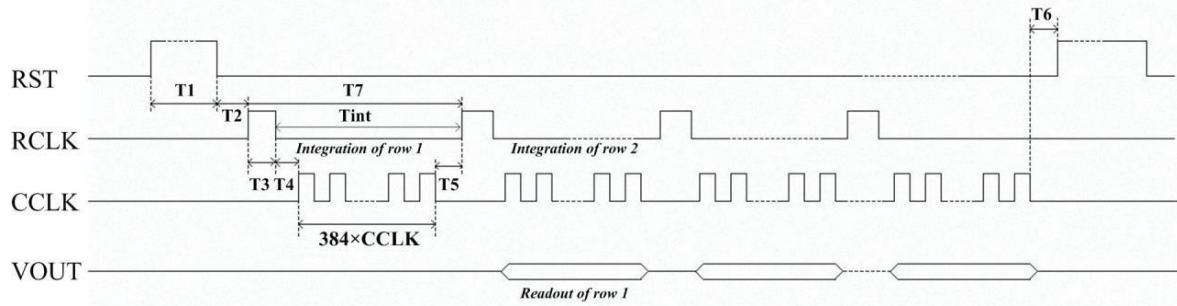
T1 > RCLK, T2 ≥ 0, T3 ≥ 4us, T4 ≥ 1.5us, T5 ≥ 1.5us, T6 ≥ 1.5us.

Integration time (Tint) is equal to the time duration of the low level of RCLK.

FIGURE 3 Recommended clock diagram for 384×288 Configuration
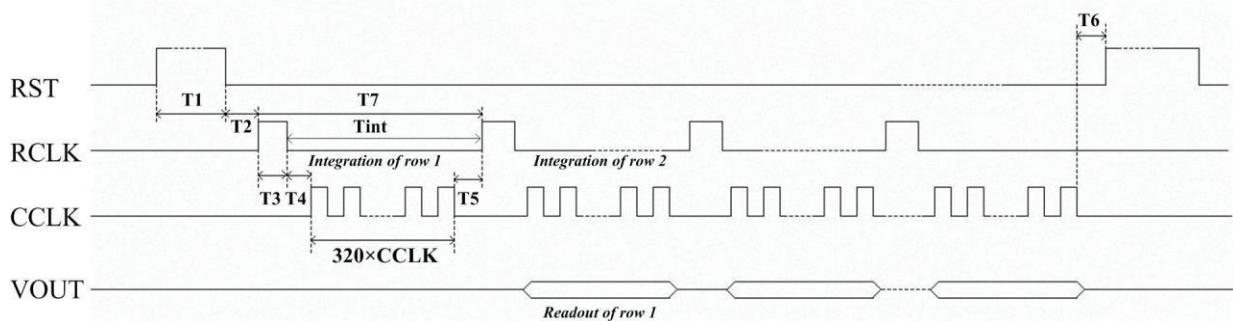
T1 > RCLK, T2 ≥ 0, T3 ≥ 4us, T4 ≥ 1.5us, T5 ≥ 1.5us, T6 ≥ 1.5us.

Integration time (Tint) is equal to the time duration of the low level of RCLK.

**FIGURE 4 Recommended clock diagram for 320×240
Configuration**

4.3 Output Conditions

The detector has two outputs, which are the analog video output and the temperature sensor output. Both output conditions are described in Table 7.

TABLE 7 Output Conditions

Pin	Symbol	Bias		Range
2	VOUT	output	variabl	0.4 -
12	TOUT	output	variabl	2.0 –

4. 4   Frame Sizing

The maximum available frame size of the **TT-1384BLD-DS** detector is 384×288, however it can also be used with a size of 320×240 by varying the value of the bit SIZE (pin 24) as well as the clock diagram. The value for operating at each frame size is set as in Table 8.

TABLE 8 Frame size selection

| Frame	Pin	SIZE set
384×28	24	5V
320×24	24	Ground
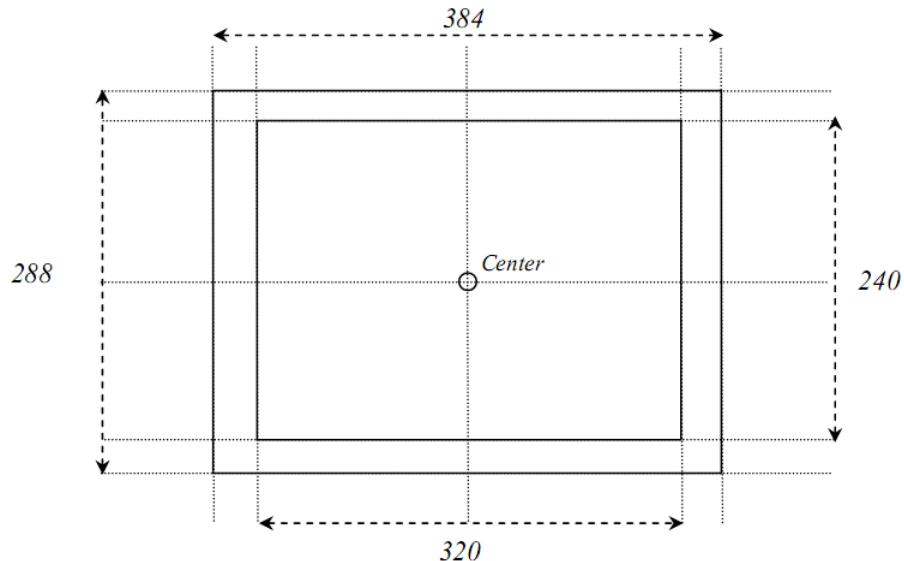
figure 5 frame sizing

4.5   Gain Control

There are three separate Pins that are used to control the CTIA capacitance, which results in the control of the gain of the CTIA. Typically smaller capacitance value will improve the NETD but will decrease the dynamic range. The selection of the capacitance is described in Table 9.

TABLE 9 Gain control selection conditions

Gain	S1 (Pin	S2 (Pin	S3 (Pin	CTIA Capacitance
0.57	5V	5V	5V	14
0.67	0V	5V	5V	12
0.80	5V	0V	5V	10
1.00	0V	0V	5V	8
1.33	5V	5V	0V	6
2.00	0V	5V	0V	4
4.00	5V	0V	0V	2

4.6   Image Flip

The image can be flipped horizontally or vertically by setting the HFLIP or VFLIP value as described in Table

10.

TABLE 10 Image flip setting

Reading Direction	HFLIP (Pin18	VFLIP (Pin
Right to left/up to	0V	5V
Right to left/down to	0V	0V
Left to right/up to	5V	5V
Left to right/down to	5V	0V

5   ENVIRONMENTAL CONDITIONS

TT-1384BLD-DS Detector is GJB-qualified (MIL-STD equivalent). The detector qualification is performed on the basis of sampling from the manufactured products and is representative of the typical manufacturing technology level. The detector should be qualified to the climatic and mechanical environmental conditions as listed in Table 11.

TABLE 11 Detector Environment Conditions

Nr	Item	Standard and Method
1	High temperature storage	GJB 1788 Method 2020
2	Low temperature storage	GJB 1788 Method 2040
3	Thermal Shocks	GJB 1788 Method 2010
4	Random vibration	GJB 1788 Method 2080
5	Shocks	GJB 1788 Method 2070

6　DELIVERY

6.1　Packing

During transportation, the detector is placed into a plastic box and wedged with conductive foam, a testing report is delivered together with each detector.

6.2　Storage

Detectors should be stored at conditions: temperature at -10℃～40℃, relative humidity is less than 70%, dry and non-corrosive environment.

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6.3　General Recommendations

Specific care should be taken in handling the DLC384 detector:
a)　Electrostatic discharge (ESD) protection
b)　Avoid directing the detector directly towards the sun, especially in the case the detector is mounted with a lens

7　APPENDIX

Three appendix sheets are attached as following
-　Sheet A: General View
-　Sheet B: Mechanical Interface
-　Sheet C: Optical Interface

Sheet A General View
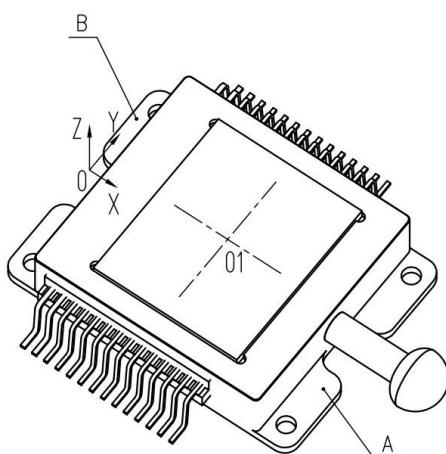
NOTE:

1-Mechanical reference OXYZ are materialised by:
　XY: Mechanical Mounting surface (A plane)
　X: Symmetry axis of the structure
　Y: Perpendicular to X axis through line B
　Z: Normal to XY plane
　O: XYZ axis center
2-O1: Optical plane center

Sheet B Mechanical Interface

Sheet C Optical Interface