ThermalTronix

TT-1160CLD-DS

Long Wave Infrared Focal Plane Array

160×120 25um Uncooled Micro-bolometer

Issue D

Product Highlights

- *a-Si micro-bolometer*
- *160×120 focal plane array*
- *Pixel pitch 25um by 25um*
- *Hermetic Vacuum package*
- *Room temperature operation with TEC*
- *Military standard qualification*
- *On-chip temperature sensor*
- *Frame rate 30Hz～100Hz*
- *Single analog output*
- *Image flip controllable*
- *Gain control selectable*

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Contents

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Glossary

CMOS	Compatible Metal Oxide Semiconductor
CTIA	Capacitance Trans-Impedance Amplifier
ESD	Electrical Static Discharge
FPA	Focal Plane Array
IR	Infrared
LWIR	Long Wave Infrared
MEMS	Micro-Electro-Mechanical Systems
NC	Not Connected
NETD	Noise Equivalent Temperature Difference
ROIC	Read Out Integrated Circuit
TEC	Thermo-Electric Cooler

1 INTRODUCTION

This document describes the operation conditions and main performance specifications of an uncooled long wave infrared focal plane array detector with reference number of **TT-1160CLD-DS**.

The **TT-1160CLD-DS** infrared detector is based on CMOS-MEMS micro-bolometer technology. The detector is a 160×120 pixels array with pixel pitch of 25um by 25um. The detector is sensitive to the long-wave infrared (LWIR) spectral range of 8um～14um.

The **TT-1160CLD-DS** infrared detector is vacuum packaged with an incorporated non-evaporable getter to maintain long-term vacuum. The temperature of the detector is controlled with a thermo-electric cooler (TEC).

The **TT-1160CLD-DS** infrared detector is read-out row-by-row and can provide a single analog output signal. The detector is typically operated under 30Hz～100Hz frame rate.

2 STRUCTURAL OVERVIEW

The **TT-1160CLD-DS** detector consists of following physical structures: hermetic sealed vacuum metal packaging, a IR filter window in the front of the packaging, a non-evaporable getter inside of the packaging to help maintain long-term vacuum level, the FPA chip with an integrated temperature sensor, a thermo-electric cooler (TEC) to stabilize the detector temperature.

2.1 Overall Dimensions

The physical structure and overall dimensions of the detector packaging are described in the Appendix (sheet A to C).

2.2 Pin-out Diagram and List

The pin-out diagram is presented in Figure 1, and the function of each pin is described in Table 1.

2.3 Infrared Filter

An infrared filter window is incorporated in the front side of the detector package; its dimensions are as following:

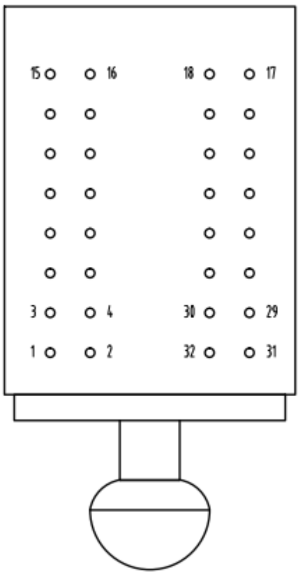
2.3.1 Dimension

The outline size of the IR filter is 9.0mm by 8.0mm; its thickness is 1.0mm.

2.3.2 Optical interface

The optical interface detail is described in the Appendix (sheet C).

PIN#	Symbol	PIN #	Symbol
15	TEC-	16	NC
13	MCLK	14	NC
11	INT	12	RST
9	SERDAT	10	DGND
7	DVDD	8	NC
5	NC	6	TOUT2
3	NC	4	NC
1	NC	2	GETTER



PIN#	Symbol	PIN #	Symbol
18	NC	17	TEC+
20	NC	19	AVDD
22	AGND	21	VOUT
24	VREF	23	TOUT1
26	NC	25	VPB
28	NC	27	VBB
30	NC	29	VPS
32	GETTER	31	VBS

FIGURE 1 Detector Pin-out Diagram

TABLE 1 Detector Pin List

Pin Nr	Symbol	Function		Pin Nr	Symbol	Function
1	NC	Not connected		17	TEC+	TEC+
2	GETTER	Getter		18	NC	Not connected
3	NC	Not connected		19	AVDD	Analog supply
4	NC	Not connected		20	NC	Not connected
5	NC	Not connected		21	VOUT	Video analog output
6	TOUT2	Temperature sensor 2 output		22	AGND	Analog ground
7	DVDD	Digital supply		23	TOUT1	Temperature sensor 1 output
8	NC	Not connected		24	VREF	Reference voltage
9	SERDAT	Serial link input data		25	VPB	Pixel biasing
10	DGND	Digital ground		26	NC	Not connected
11	INT	Integration time		27	VBB	Blind pixel biasing
12	RST	Reset		28	NC	Not connected
13	MCLK	Main clock		29	VPS	Pixel ground
14	NC	Not connected		30	NC	Not connected
15	TEC-	TEC-		31	VBS	Blind pixel supply
16	NC	Not connected		32	GETTER	Getter

Note: the NC pins can **NOT** be connected to any signal bus such as the ground etc.

2.4 TEC

TABLE 2 Bias Requirements For The TEC

Pin Nr	Symbol	Absolute Max Rating
15	TEC-	

17	TEC+	Voltage:2.8V Current: 1.8A

The temperature stabilization is required to be 10mK.

The stabilized temperature of the detector is typically set 10K～20K above the ambient temperature.

2.5 Temperature Sensor

Two CMOS temperature sensors are integrated in the FPA ROIC chip, and two separate analog output TOUT1 and TOUT2 are provided, the functions of the two TOUT are equivalent, each one can be used to control the TEC **(the non-used TOUT should be floated, can NEVER be connected to the ground).**

A typical TOUT versus the detector chip temperature relationship is shown in Figure 2. The sensitivity of the temperature sensor is about -7.85 mV/K. TOUT is about 2.70 V for an FPA temperature of 25°C.

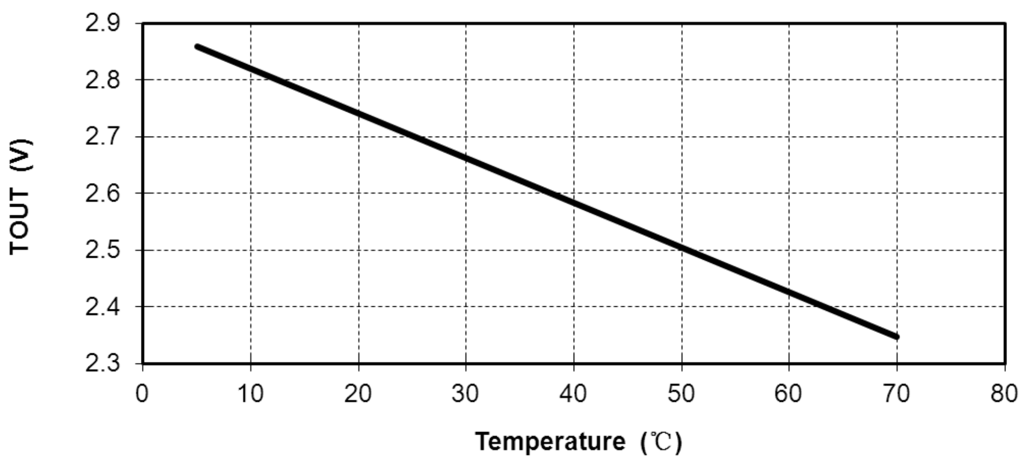


FIGURE 2 Typical temperature sensor output TOUT characteristics

2.6 Vacuum and Getter

The **TT-1160CLD-DS** detector is required to operate under high vacuum condition. A non-evaporable getter is integrated in the packaging to maintain the long-term vacuum level. The getter can be electrically re-activated when the performance of the detector is degraded due to the vacuum level degradation. The getter activation is performed by supplying a constant current to the two pins of the getter as shown in Table 3. Re-active the getter by the customer is not recommended.

TABLE 3 Getter Re-activation Conditions

Pin Nr	**Symbol**	**Current**	**Time**
2/32	Getter	4.0A±0.1A	10min

2.7 Weight

The total weight of the **TT-1160CLD-DS** detector is less than 7g.

2.8 Operating Temperature

The operating temperature range of the **TT-1160CLD-DS** detector is from -40°C to +60°C. A heat sink condition with typical thermal resistance of 4K/W is required between the packaging base plate and the ambient, especially when the detector is operated at the high end of the temperature range.

2.9 Storage Temperature

The storage temperature range of the **TT-1160CLD-DS** detector is from -40℃ to +85℃.

3 PERFORMANCE SPECIFICATIONS

A detector test report is provided with each delivered detector by the manufacturer, which contains testing results of the responsivity, temporal NETD and operability.
The definitions of several parameters are further explained as following.

3.1 Responsivity

The detector responsivity is not a fixed performance specification parameter, the value supplied the test report is a measured value under the certain biasing and test conditions.

3.2 Operability specification

3.2.1 Non-operating pixel

A pixel is defined as a “non-operating” if:

- its responsivity is less than 0.8x average responsivity or larger than 1.2x average responsivity; or
- its NETD is larger than 1.5x average NETD;

3.2.2 Non-operating Row

A row is considered as non-operating if larger than 50% of the pixels are non-operating.

3.2.3 Non-operating Column

A column is considered as non-operating if larger than 50% of the pixels are non-operating.

3.2.4 Operability Specification

The operability of the delivered detector should meet the requirement in Table 4.

TABLE 4 Operability Specification

Non-operating row or column	0
Non-operating pixels	≤1%
Operability	≥99%

4 ELECTRICAL INTERFACE

4.1 Operation Bias Voltages

To properly operate the **TT-1160CLD-DS**, various bias voltages should be supplied to each pin as specified in Table 5.

TABLE 5 Operation Bias Conditions

Pin Nr	Symbol	Bias Type		Optimum Value	Range	Max Current	Max RMS Noise
7	DVDD	Input	Fixed	5V±300mV	—	5mA	<100mV
10	DGND	Input	Fixed	0V	—	5mA	—
19	AVDD	Input	Fixed	5V±100mV	—	20mA	2uV(1Hz～1KHz) 5uV(1Hz～10KHz) 100uV(1Hz～10MHz)
22	AGND	Input	Fixed	0V	—	20mA	—
24	VREF	Input	Fixed	2.4V±25mV	—	1mA	<100uV
25	VPB	Input	Tunable	Given in the test report	2V-5V	100uA	2uV(1Hz～1KHz) 5uV(1Hz～10KHz) 100uV(1Hz～10MHz)
27	VBB	Input	Fixed	1.6V	—	100uA	2uV(1Hz～1KHz) 5uV(1Hz～10KHz) 100uV(1Hz～10MHz)
29	VPS	Input	Fixed	0V	—	5mA	—
31	VBS	Input	Tunable	Given in the test report	2V-5V	5mA	2uV(1Hz～1KHz) 5uV(1Hz～10KHz) 100uV(1Hz～10MHz)

VPB、VBS can be adjusted to optimize the detector performance within the above range.

Note：Special Requirements for Supplying the Bias Voltages (the detector could be severely damaged if the following instructions are not followed):

1） When supply the bias voltages, it is required that the VPB is supplied last, when all the other signals and bias have been supplied and stabilized;

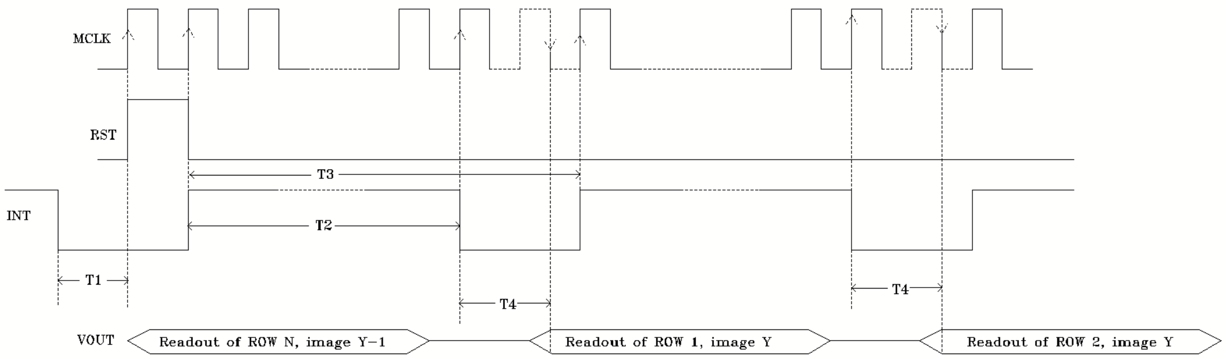
2） When power off the detector. it is required that the VPB is turned off first, all the other signals and bias voltage can be turned off only after the VPB has been off;

3） If need to change SERDAT input to achieve serial link control then the detector is actively biased, it is required to turn the VPB signal off firstly, then change SERDAT, and turn on the VPB again.

4.2 Pulse Voltage and Clock Diagram

TABLE 6 Pulse Voltages

Pin Nr	Symbol	Pulse Type		Low Level			High Level		
				Min	Typical	Max	Min	Typical	Max
13	MCLK	Input	5V TTL	-0.3V	0V	0.3V	4.7V	5V	5.5V
11	INT	Input	5V TTL	-0.3V	0V	0.3V	4.7V	5V	5.5V
12	RST	Input	5V TTL	-0.3V	0V	0.3V	4.7V	5V	5.5V
9	SERDAT	Input	5V TTL	-0.3V	0V	0.3V	4.7V	5V	5.5V



T1≥15TMCLK， 15TMCLK≤T2 (Integration time)≤160 TMCLK, T3≥(160+17)TMCLK， T4=18.5TMCLK

FIGURE 3 Clock Diagram for 160×120 Configuration

4.3 Serial Control

The serial control bus is developed for infrared imagers. SERDAT（Pin #9）is serial control bus.

4.3.1 SERDAT=0V

a) Recommended control mode,
b) CTIA Capacitance is 6pF ,
c) The image is not flipped,
d) Window size is 160×120.

4.3.2 SERDAT input

SERDAT is a 17bits control signal defined as in Table 7. The main feature of the serial interface include：

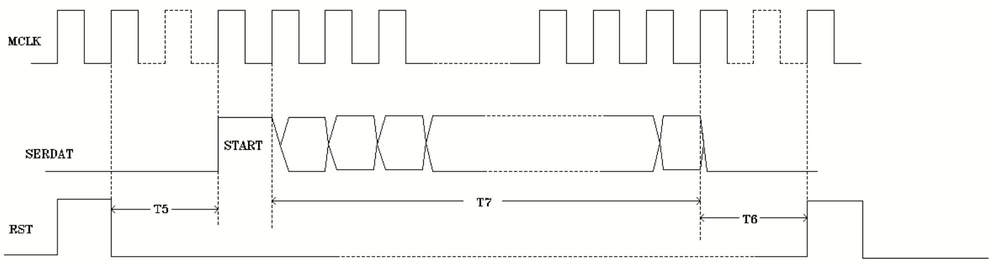
a) CTIA gain value：GAIN,
b) Image flip：HFLIP、VFLIP,
c) Windowing：SIZE.

SERDAT can be applied by each frame or just once.
To activate the serial control bus, the first bit named START needs to be set at "1" i.e high level.

The clock frequency of SERDAT is governed by the Master Clock (MCLK). Data will be taken into account if START bit is at high level. Data must change during rising edge of MCLK and will be taken into account at the falling edge of the next RST. The timing diagram of SERDAT is shown in Figure 4.

TABLE 7 Serial Link Instruction

Position	Length (in bit number)	Name	Format	Example Value
1	1	START	binary	1
2	10	Reserved	binary	0000000000
3	3	Gain	binary	111
4	1	HFLIP	binary	1
5	1	VFLIP	binary	1
6	1	SIZE	binary	0



T5≥1TMCLK， T6≥1TMCLK， T7=16TMCLK

FIGURE 4 SERDAT Timing Diagram TABLE 8 Main feature of serial interface

Name	Value	Description
Gain	000	2pF
	100	4pF
	010	6pF
	110	8pF
	001	10pF
	101	12pF
	011	14pF
	111	16pF
HFLIP	1	Normal (Scanning from right to left)
	0	Horizontal flip (Scanning from left to right)
VFLIP	1	Normal (Scanning from up to down)
	0	Vertical flip (Scanning from down to up)
SIZE	1	168×128
	0	160×120

4.4 Output Characteristics

The detector contains two type of outputs. VOUT is the analog video output; TOUT1 and TOUT2 are the temperature sensor output. The outputs are described in Table 9.

TABLE 9 Outputs

Pin Nr	Symbol	Output Type		Range
21	VOUT	Output	variable	0.4V～4.0V
23	TOUT1	Output	variable	2.0V～3.3V
6	TOUT2	Output	variable	2.0V～3.3V

5 ENVIRONMENTAL CONDITIONS

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TT-1160CLD-DS detector is GJB-qualified (MIL-STD equivalent). The detector qualification is performed on the basis of sampling from the manufactured products and is representative of the typical manufacturing technology level. The detector should be qualified to the climatic and mechanical environmental conditions as listed in Table 10.

TABLE 10 Environment Conditions

Nr	**Item**	**Standard and Method**
1	High temperature storage	GJB 1788 Method 2020
2	Low temperature storage	GJB 1788 Method 2040
3	Thermal Shocks	GJB 1788 Method 2010
4	Random vibration	GJB 1788 Method 2080
5	Shocks	GJB 1788 Method 2070

6 DELIVERY

6.1 Packing

During transportation, the detector is placed into a plastic box and wedged with conductive foam, a testing report is delivered together with each detector.

6.2 Storage

Detectors should be stored at conditions: temperature at -10℃～40℃, relative humidity is less than 70%, dry and non-corrosive environment.

6.3 General Recommendations

Specific care should be taken in handling the **TT-1160CLD-DS** detector:

a) Electrostatic discharge (ESD) protection

b) Avoid directing the detector directly towards the sun, especially in the case the detector is mounted with a lens

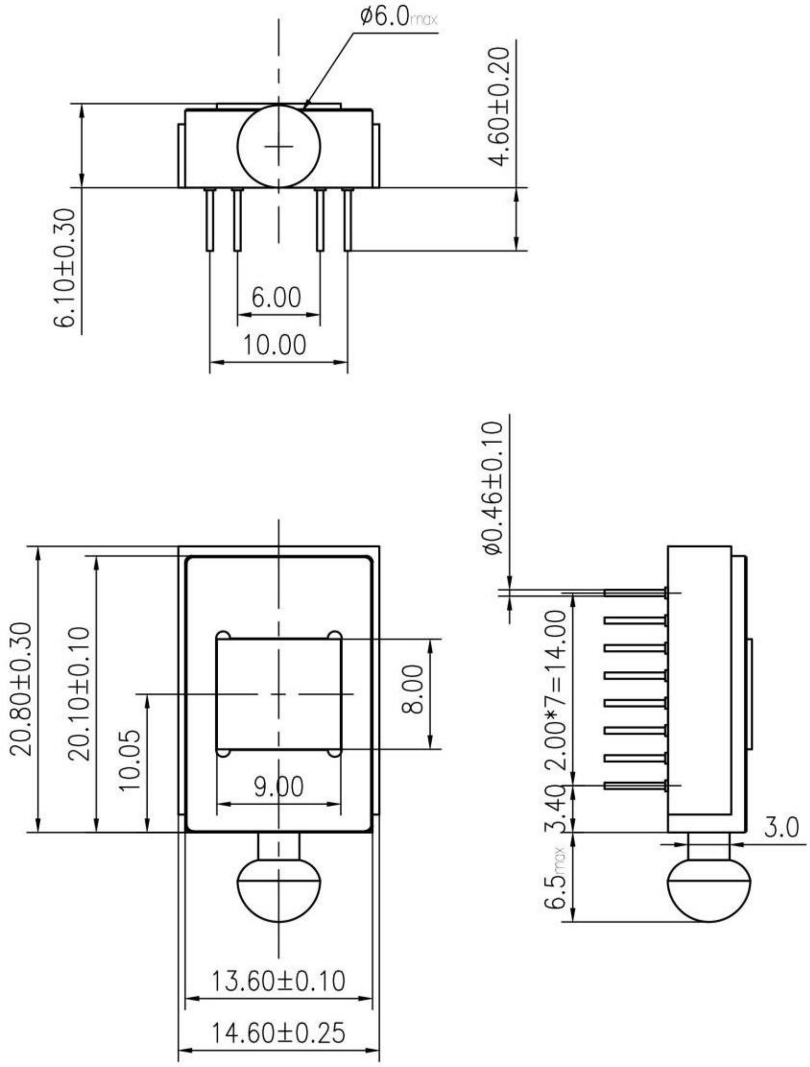
7 APPENDIX

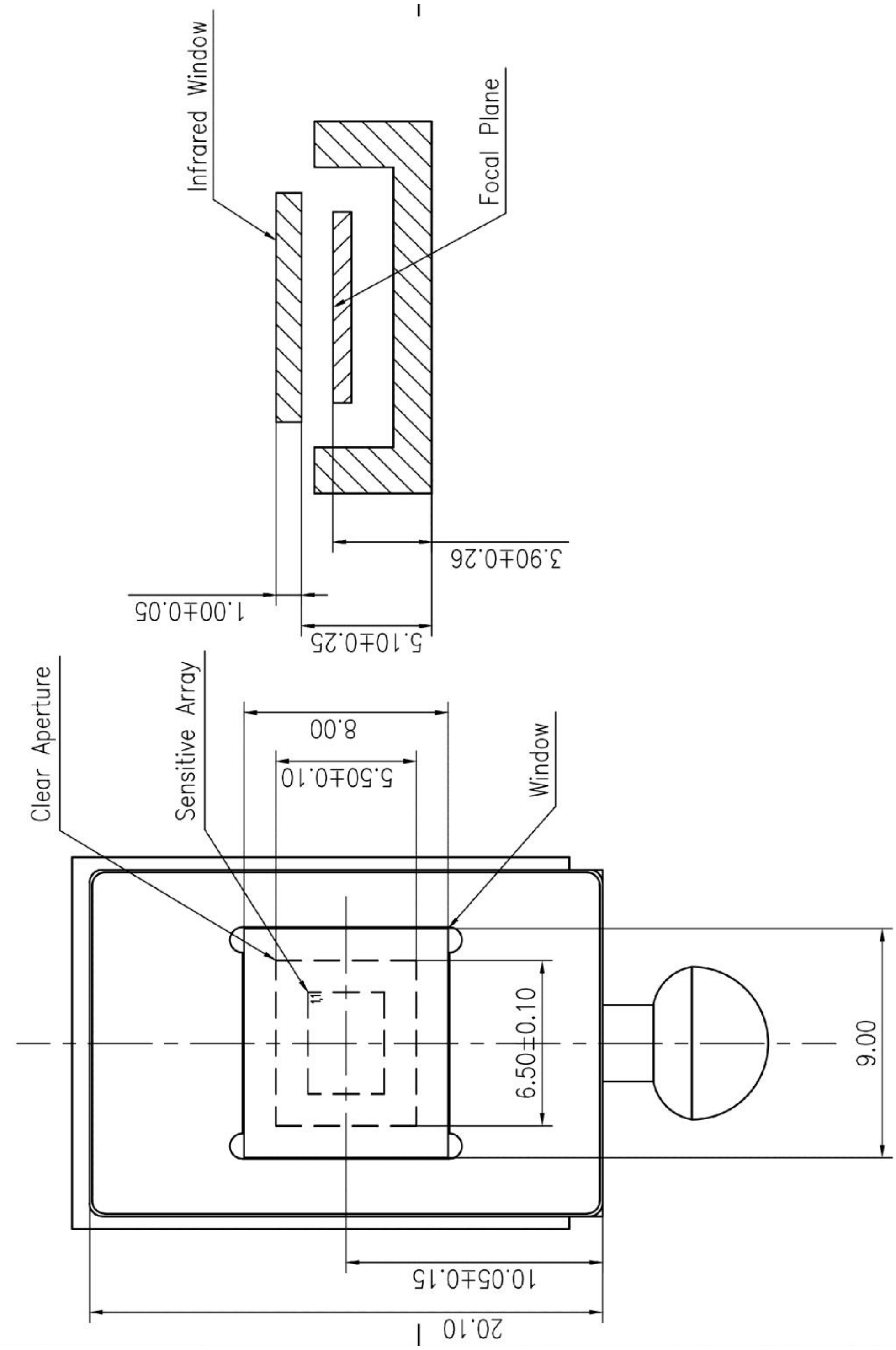
a) Sheet A：Mechanical Interface

b) Sheet B：Optical Interface

c) Sheet A Mechanical Interface

Sheet B Optical Interface




Infrared Window
Focal Plane
3.90±0.26
1.00±0.05
5.10±0.25
Clear Aperture
Sensitive Array
Window
8.00
5.50±0.10
6.50±0.10
9.00
10.05±0.15
20.10